CLAIMS

1. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

a first pad; and

a programmable I/O circuit (PIC) associated with the first pad, wherein the PIC comprises:

a first output buffer adapted to present a first outgoing signal at the first pad; and

a first transmission gate connected between the first pad and the first output buffer, wherein:

the first transmission gate is adapted to be closed when the first output buffer is selected to present the first outgoing signal at the first pad; and

the first transmission gate is adapted to be open when the first output buffer is selected not to present the first outgoing signal at the first pad, wherein capacitive loading at the first pad due to the first output buffer is lower when the first transmission gate is open than when the first transmission gate is closed.

2. (original) The invention of claim 1, wherein:

a first side of the first transmission gate is connected directly to the first pad; and

a second side of the first transmission gate is connected directly to an output of the first output buffer.

3. (original) The invention of claim 1, wherein the first output buffer is a single-ended output buffer.

4. (original) The invention of claim 1, wherein the PIC further comprises:

one or more other output buffers, each adapted to present an other outgoing signal at the first pad; and

one or more other transmission gates, each connected between the first pad and a corresponding other output buffer, wherein:

each other transmission gate is adapted to be closed when the corresponding other output buffer is selected to present the corresponding other outgoing signal at the first pad; and

each other transmission gate is adapted to be open when the corresponding other output buffer is selected not to present the corresponding other outgoing signal at the first pad, wherein capacitive loading at the first pad due to the other output buffer is lower when the other transmission gate is open than when the other transmission gate is closed.

5. (original) The invention of claim 1, wherein the first transmission gate comprises a plurality of switch devices connected in parallel between first and second sides of the first transmission gate.

6. (original) The invention of claim 5, wherein the plurality of switch devices are individually controllable.

7. (original) The invention of claim 6, wherein the plurality of switch devices are adapted to be individually and selectively controlled to compensate for variation in switch-device resistance due to at least one of process and temperature.

8. (original) The invention of claim 1, wherein:

the programmable device is an FPGA;

a first side of the first transmission gate is connected directly to the first pad;

a second side of the first transmission gate is connected directly to an output of the first output buffer;

the first output buffer is a single-ended output buffer;

the first transmission gate comprises a plurality of switch devices connected in parallel between first and second sides of the first transmission gate, wherein the plurality of switch devices are adapted to be individually and selectively controlled to compensate for variation in switch-device resistance due to at least one of process and temperature; and

the PIC further comprises:

one or more other output buffers, each adapted to present an other outgoing signal at the first pad; and

one or more other transmission gates, each connected between the first pad and a corresponding other output buffer, wherein:

each other transmission gate is adapted to be closed when the corresponding other output buffer is selected to present the corresponding other outgoing signal at the first pad; and

each other transmission gate is adapted to be open when the corresponding other output buffer is selected not to present the corresponding other outgoing signal at the first pad, wherein capacitive loading at the first pad due to the other output buffer is lower when the other transmission gate is open than when the other transmission gate is closed.

9. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

a plurality of pads;

a programmable I/O circuit (PIC) associated with the pads, wherein the PIC comprises:

a plurality of single-ended output buffers, each associated with at least one pad; and

at least one double-ended output buffer associated with at least two pads; and

a transmission gate connected between each single-ended output buffer and its at least one associated pad.

10. (currently amended) The invention of claim [[9]] 20, wherein each single-ended output buffer is associated with at least two pads, wherein a transmission gate is connected between each single-ended output buffer and each of its at least two associated pads.

11. (original) The invention of claim 9, wherein the PIC further comprises a plurality of input receivers, each associated with at least one pad.

12. (original) A programmable device having programmable input/output (I/O) circuitry and programmable logic connected to receive incoming signals from and provide outgoing signals to the I/O circuitry, the programmable device comprising:

a first pad; and

a programmable I/O circuit (PIC) associated with the first pad, wherein the PIC comprises:

a low-speed output buffer adapted to present a first outgoing signal at the first pad;

a first transmission gate connected between the first pad and the first low-speed output buffer, the transmission gate having a lower output capacitance than the low-speed buffer; and

a high-speed output buffer adapted to present a second outgoing signal at the first pad.

13. (original) The invention of claim 12, wherein the low-speed buffer is a single-ended output buffer and the high-speed buffer is a double-ended output buffer.

14. (new) The invention of claim 1, wherein:
the programmable device further comprises a second pad; and
the PIC further comprises a second transmission gate connected between the first output buffer and the second pad.

15. (new) The invention of claim 14, wherein the PIC further comprises:
one or more other output buffers;
a first set of one or more other transmission gates, each connected between the first pad and a corresponding other output buffer; and
a second set of one or more other transmission gates, each connected between the second pad and a corresponding other output buffer.

16. (new) The invention of claim 1, wherein:
the programmable device further comprises a second pad; and
the PIC further comprises a double-ended output buffer associated with the first and second pads.

17. (new) The invention of claim 16, wherein:
the first output buffer is a single-ended output buffer;
the programmable device further comprises third and fourth pads; and
the PIC further comprises:
a second transmission gate connected between the first single-ended output buffer and the third pad;
a first set of one or more other single-ended output buffers;
a second set of one or more other single-ended output buffers;
a first set of one or more transmission gates, each connected between the first pad and a corresponding single-ended output buffer of the first set;
a second set of one or more transmission gates, each connected between the second pad and a corresponding single-ended output buffer of the second set;
a third set of one or more transmission gates, each connected between the third pad and a corresponding single-ended output buffer of the first set; and
a fourth set of one or more transmission gates, each connected between the fourth pad and a corresponding single-ended output buffer of second first set.

18. (new) The invention of claim 1, wherein:
the first output buffer is a low-speed output buffer; and
the PIC further comprises a high-speed output buffer adapted to present a second outgoing signal at the first pad.

19. (new) The invention of claim 18, wherein:
the low-speed output buffer is a single-ended output buffer; and
the high-speed output buffer is a double-ended output buffer.

20. (new) The invention of claim 9, wherein at least one single-ended output buffer is associated with at least two pads, wherein a transmission gate is connected between the at least one single-ended output buffer and each of its at least two associated pads.

21. (new) The invention of claim 9, wherein the at least one double-ended output buffer and a first single-ended output buffer are both associated with a first pad.

22. (new) The invention of claim 21, wherein one or more other single-ended output buffers are also associated with the first pad.

23. (new) The invention of claim 21, wherein the at least one double-ended output buffer and one or more other single-ended output buffers are all associated with a second pad.

24. (new) The invention of claim 12, wherein:
the programmable device further comprises a second pad; and
the PIC further comprises a second transmission gate connected between the low-speed output buffer and the second pad.